

1 1. A method comprising:
2 forming a tapered electrode for a phase-change
3 memory cell; and
4 forming a trench using the tapered electrode as a
5 mask.

1 2. The method of claim 1 including covering said
2 tapered electrode with an insulator.

1 3. The method of claim 1 including forming a pair of
2 tapered electrodes for a pair of adjacent phase-change
3 memory cells, covering the electrodes with an insulator and
4 forming a trench between the covered tapered electrodes as
5 a mask.

1 4. The method of claim 1 including self-aligning the
2 trench to the tapered electrode.

1 5. The method of claim 1 including forming a tapered
2 electrode by isotropically etching.

1 6. The method of claim 1 including forming junctions
2 below said tapered electrode.

1 7. The method of claim 6 including forming a
2 plurality of layers of different doping levels.

1 8. The method of claim 7 including forming said
2 layers by ion implantation.

1 9. The method of claim 7 including etching said
2 layers using the same isotropic etch used to form said
3 tapered electrode.

1 10. The method of claim 9 including forming a tapered
2 substrate portion below said tapered electrode.

1 11. The method of claim 10 including forming a
2 conical-shaped substrate portion covered by said tapered
3 electrode.

1 12. The method of claim 10 including covering said
2 tapered substrate portion with an insulator and anisotropic
3 etching said covered tapered substrate portion.

1 13. A phase-change memory comprising:
2 a tapered lower electrode; and
3 a trench on either side of said tapered
4 electrode.

1 14. The memory of claim 13 including an insulator
2 over said electrode.

1 15. The memory of claim 13 including a substrate
2 under said tapered electrode, said substrate including a
3 lower portion and a tapered upper portion.

1 16. The memory of claim 15 wherein said insulator
2 covers said tapered substrate portion.

1 17. The memory of claim 16 wherein said lower
2 substrate portion is free of said insulator.

1 18. The memory of claim 14 wherein said trenches are
2 self-aligned to said tapered electrode.

1 19. The memory of claim 14 wherein said tapered
2 electrode is conical.

1 20. The memory of claim 15 wherein said tapered
2 substrate portion includes a first region of a first
3 conductivity type over a second region of a second
4 conductivity type.

1 21. The memory of claim 20 wherein said first type is
2 P type and said first region is sandwiched between said
3 second region and said electrode.

1 22. The memory of claim 21 including a buried
2 wordline formed in said upper portion.

1 23. A method comprising:
2 forming a conical structure over a substrate; and
3 using said conical structure as a mask to form a
4 trench.

1 24. The method of claim 23 including forming a
2 conical structure including a tapered electrode at the top
3 of said conical structure.

1 25. The method of claim 23 including forming a
2 plurality of layers in said conical structure of different
3 conductivity types.

1 26. The method of claim 24 including forming layers
2 in said conical structure of the same conductivity type but
3 different doping levels.

1 27. The method of claim 23 including forming a phase-
2 change material over said conical structure.

1 28. The method of claim 27 including forming an
2 electrode over said phase-change material.

1 29. The method of claim 23 including covering said
2 conical structure with an insulator.

1 30. The method of claim 29 including anisotropically
2 etching said covered conical structure.

1 31. A phase-change memory comprising:
2 a substrate;
3 a conical structure formed over said substrate,
4 said conical structure including an electrode;
5 a trench self-aligned to said conical structure;
6 and
7 a phase-change material in contact with said
8 electrode.

1 32. The memory of claim 31 wherein said conical
2 structure includes a plurality of layers of different
3 conductivity types.

1 33. The memory of claim 32 wherein said conical
2 structure includes a conductive line.

1 34. The memory of claim 31 including an insulator
2 covering said conical structure.

1 35. The memory of claim 31 including two trenches
2 self-aligned to said conical structure.